REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made."**

Reconsideration of the application is respectfully requested. Applicants have addressed every objection and ground for rejection, in the Office Action, and believe that the application is now in condition for allowance.

Figs. 1-3 have been amended to include a legend "Prior Art," as required by the Examiner. A separate letter to the Draftsman is enclosed herewith.

Claims 1-13 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Youn. Applicants respectfully traverse this rejection, because the cited reference does not disclose or suggest the driver which is divided into a plurality of blocks, so as to divide the liquid crystal display panel into sections arranged side by side, as now recited in claim 1. These blocks simultaneously supply the liquid crystal display panel with display signals that have been supplied to the blocks.

The Youn reference relates to a liquid crystal display, and discloses a pair of data drivers 2a and 2b which are provided one on each opposing two sides of a liquid display panel 1. The signal lines D_1-D_{2n-1} from the data driver 2a are arranged alternately or interdigitated with those D_2-D_{2n} of the data driver 2b (see Fig. 2) across the entire liquid crystal display panel.

In contrast, the claimed data driver is divided into a plurality of blocks each of which separate the liquid display panel into corresponding sections that are arranged side by side, and not alternately as in the Youn reference. This is shown in Fig. 4, where the signal lines from each of the blocks 46A-46D are provided entirely within their corresponding sections of the display panel. For this reason, claim 1 and its dependent claims 2-13 are believed to be allowable over the Youn references.

New claims 14-17 describe features of a data driver which are similar to those of claim 1, and are also believed to be allowable for the reason given with respect to claim 1.

The above amendments to the claims, in view of the foregoing remarks, are believed to place the present application in condition for allowance, which is respectfully requested. The Examiner should contact Applicants' undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning on page 1, line 13 has been amended as follows:

A liquid crystal display panel is as small as a few inches and has relatively small delay of time due to the resistances of interconnection lines.

The paragraph beginning on page 3, line 18 has been amended as follows:

However, when the panel 16 has a large size of 10 inches or more, each line of the 24-bit data buses 22 has a resistance of 10 kΩ or more. Additionally, the resistance of the display signal lines 30 cannot be neglected. The resistance of the display signal lines 30 can be reduced if an increased number of lines 30 is used, as shown in Fig. 3. The structure shown in Fig. 3 employs 300 display signal lines to which display signals D1-D300 are respectively applied. The display signal lines 42 can be driven by a general – purpose data driver IC marketed. [An] When a increased number of display signal lines is used, the display data can be written onto the data buses 22 for a longer time. Hence, the width of each of the display signal lines 42 can be reduced. However, the total width of the display signal lines 42 is approximately equal to 6.0 mm. This increases the size of the peripheral circuits with regard to the panel 16.

The paragraph beginning on page 4, line 31 has been amended as follows:

The above object of the present invention is achieved by a liquid crystal display device comprising: a liquid crystal display panel; a data driver connected to the liquid crystal display panel; and a gate driver connected to the liquid crystal display panel. The data driver [being] is divided into a plurality of blocks, which simultaneously supply the liquid crystal display panel with display signals respectively supplied thereto. Hence, each of the blocks has a reduced number of display signal lines, which reduces an area for arranging the display signal lines. Hence, the cross-coupling capacitance can be reduced.

The paragraph beginning on page 9, line 18 has been amended as follows:

Eight-bit signals 86A, 86B and 86C are applied to the respective eight-bit digital latch circuits of the same group from the display signal supply device 114. The signal 86A consists of eight bits of display data R. The signal 86B consists of eight bits of display data B. The signal 86C consists of eight bits of display data C. The three latch circuits 88 of the same group are supplied with the shift pulse from the shift register 80 and simultaneously latch the eight-bit signals 86A-86C, respectively. Then, the next three latch circuits 88 of the same group are supplied with the shift pulse from the shift register 80 and simultaneously the eight-bit signals 86A-86C, respectively. In the above manner, the digital eight-bit latch circuits 88 are sequentially selected [every three ones]. When all the 300 latch circuits 88 have latched the corresponding eight-bit digital signals, a latched enable signal LE is applied to the digital eight-bit latch circuits 92, which

simultaneously latch the eight-bit display signals from the corresponding latch circuits 88.

The paragraph beginning on page 12, line 31 has been amended as follows:

After the select signal rd is applied, the latch enable signal LE is activated, and the 300 bits of display data latched in the circuit 88 are latched in the digital eight-bit latch circuits 92 shown in Fig. 8. When the latch enable signal LE is high and active, all the output select signals ra-rd are low and [is] are thus inactive. This is intended to satisfy that the general driver IC device 76 is required to inhibit the device 76 from latching next data for a given time equal to, for example, 5 clocks while the previous data is output.

The paragraph beginning on page 18, line 37 has been amended as follows:

Fig. [18] 19 is a circuit diagram of each of the D/A converters 94, which converts the eight-bit digital signal into a corresponding analog signal. The D/A converter 94 includes transistors [140-140] 140-147 which implement resistors of different resistance values, and gate transistors 150-157. The transistors 140-147 have different channel widths W0-W7, which realize the different resistance values. For example, the channel width WO is the shortest, and the channel width W7 is the longest. The drains of the transistors 140-147 are supplied with the power supply voltage VDD. The gates of the transistors 140-147 are supplied with a high-level bias signal, so that all the transistors 140-147 are ON. The source of the transistors 140-147 are connected to

the drains of the transistors 150-157. The gates of the transistors 150-157 are supplied with the respective bits of the eight-bit digital input signal, and the sources thereof are grounded via a resistor R and are connected to an output terminal 160. The current flowing in the resistor R depends on which transistors are turned on in response to the eight-bit digital input signal. The voltage of the end of the resistor R1 depends on the magnitude of the current flowing in the resistor R.

In the Claims:

Claim 1 has been amended and claims 14-17 have been added as follows:

1. (Amended) A liquid crystal display device including data driver and a gate driver, comprising:

a liquid crystal display panel; and

[a data driver connected to the liquid crystal display panel; and

a gate driver connected to the liquid crystal display panel,]

a substrate on which said liquid crystal display panel, and said data driver, and said gate driver are integrally formed,

the data driver being divided into a plurality of blocks so as to divide the liquid crystal display panel into sections arranged side by side, which simultaneously supply the liquid crystal display panel with display signals respectively supplied thereto.

14. (New) A liquid crystal display device including a data driver and a gate driver, comprising:

a liquid crystal display panel; and

groups of signal lines for carrying display signals,

the data driver being divided into a plurality of blocks from which the groups of signal lines extend over corresponding partial areas of the liquid crystal display panel so that each of the groups of signal lines is associated with a respective one of the blocks of the data driver.

15. (New) A liquid crystal display device including a data driver and a gate driver, comprising:

a liquid crystal display panel, and

signal lines extending from the data driver,

the data driver and the signal lines being divided into a plurality of blocks so that the divided signal lines extending from one of the plurality of blocks extend over a corresponding divided area of the liquid crystal display panel,

said divided signal lines in each of the plurality of blocks being adjacent to each other.

16. (New) A liquid crystal display device including a data driver and a gate driver, comprising:

a liquid crystal display panel; and

a substrate on which said liquid crystal display panel, said data driver, and said gate driver are integrally formed,

the data driver being divided into a plurality of blocks arranged side by side along an edge of the liquid crystal display panel.

17. (New) The liquid crystal display panel as claimed in claim 16, wherein said data driver comprises polysilicon transistors.

FIG. 1 (PRIOR ART)

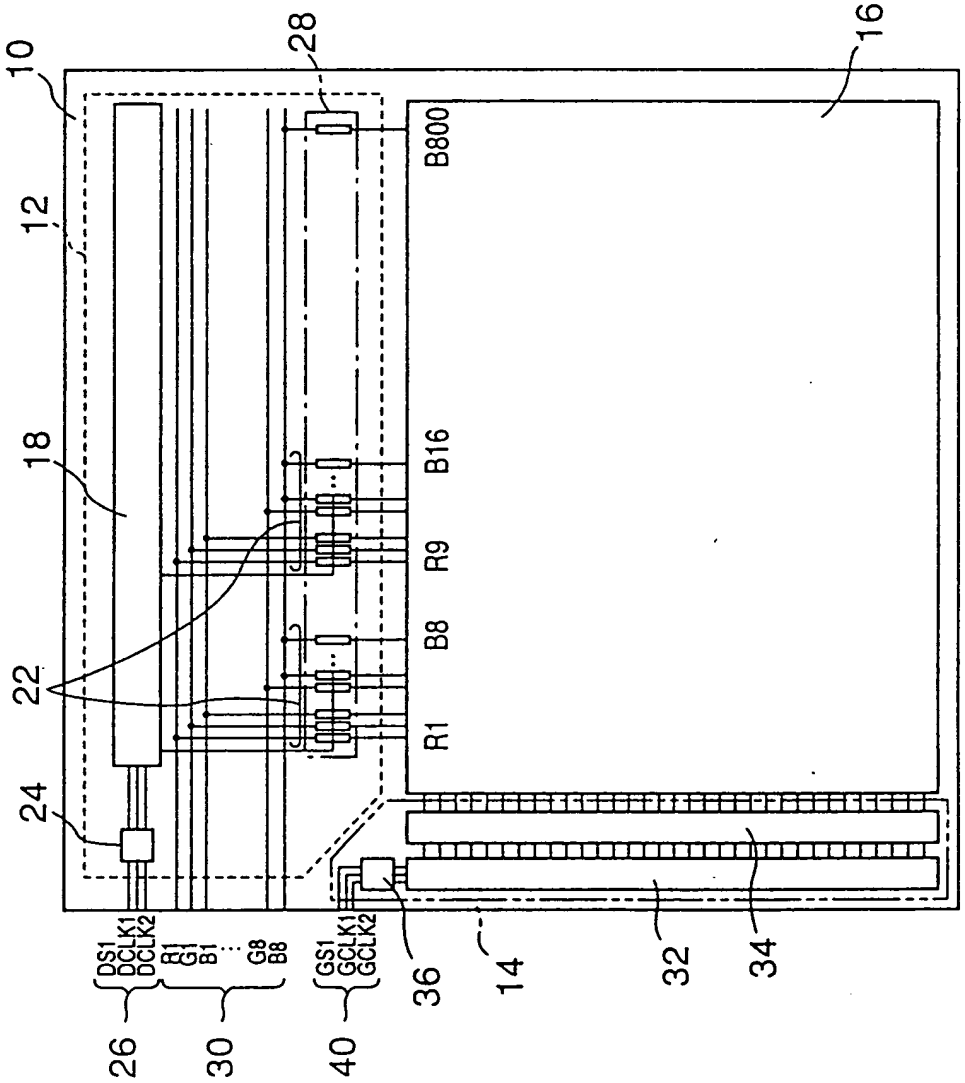

FIG. 2
(PRIOR ART)

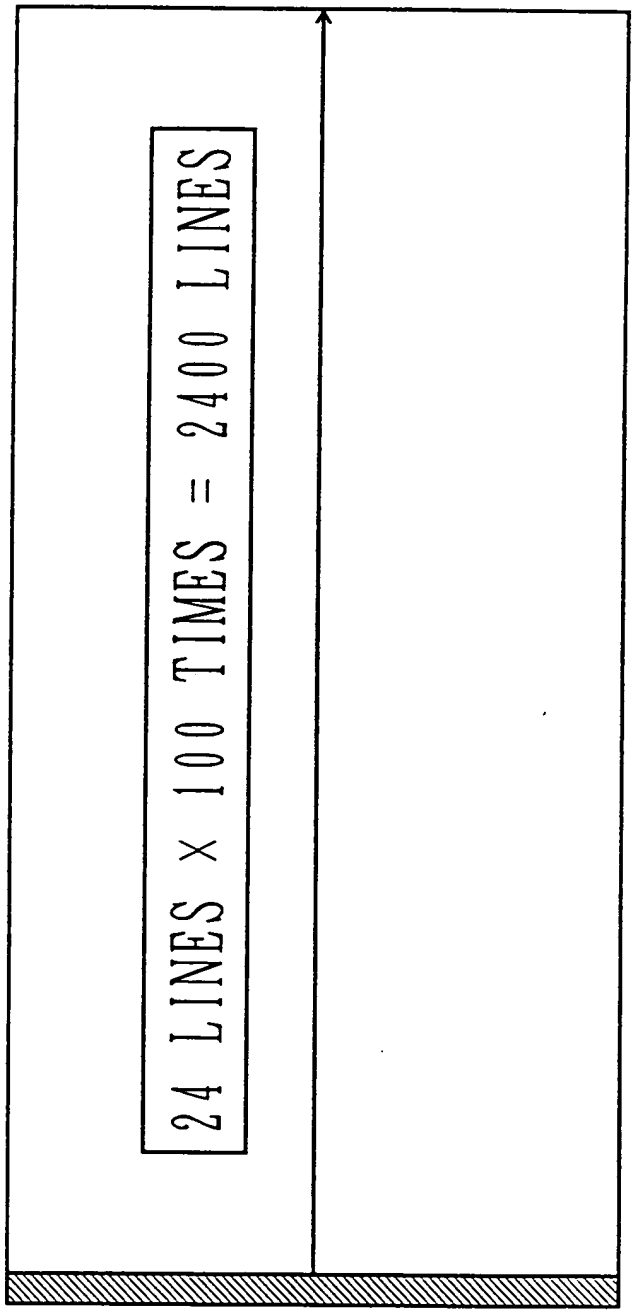

FIG. 3 (PRIOR ART)